nent count and thus lowers power dissipation. This yields the benefit of longer usage time per battery replacement or charging; reduced weight and size by use of fewer and/or smaller batteries; reduced thermal and electromagnetic emissions; and increased reliability. The system is ideal for battery-operated processor-based equipment, where it is desirable to minimize battery size so that the equipment can be made small and lightweight. The reduction is due to the fact that the functional units are not kept on when they are not needed. Since CMOS technology is used, power is only consumed when a functional unit is changing state (i.e., switching). Since a functional unit is "off" when it is prevented from changing state, negligible power is consumed by that functional unit. This means that a functional unit that is off does not consume power, which results in the power consumption reduction. Since power consumption is reduced, the heat dissipation requirements and associated packaging of the system is reduced. In addition, when a battery source is used, it can be made smaller for a given operational period of time. Furthermore, because power consumption is reduced, the line width of power supply buses can also be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

[0015] **FIG. 1** is a block diagram of a single chip wireless communications integrated circuit.

[0016] **FIG. 2** is a block diagram of a clock controller embodiment.

[0017] **FIG. 3** is a block diagram of a first embodiment to conserve power consumption for a plurality of processing units operating in parallel.

[0018] **FIG. 4** is a block diagram of a second embodiment to conserve power consumption for a plurality of processing units operating in parallel.

[0019] **FIG. 5** is a block diagram of a third embodiment to conserve power consumption for a plurality of processing units operating in parallel.

[0020] **FIG. 6** is a block diagram of a fourth embodiment to conserve power consumption for a plurality of processing units operating in parallel.

[0021] **FIG. 7** is a block diagram of a portable computer system in accordance with the present invention.

DESCRIPTION

[0022] Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

[0023] **FIG. 1** shows a block diagram of a multi-mode wireless communicator device **100** fabricated on a single silicon integrated chip. In one implementation, the device **100** is an integrated CMOS device with radio frequency (RF) circuits, including a cellular radio core **110**, a short-range wireless transceiver core **130**, and a sniffer **111**, along side digital circuits, including a reconfigurable processor core **150**, a high-density memory array core **170**, and a router **190**. The cellular core **110**, the wireless transceiver core **130**, and the processor core **150** receive clock signals from a clock controller **140**. By clocking the cores **110**, **130** and **150** using a common reference clock signal, the system simplifies the maintenance of clock signal integrity and minimizes the potential for errors from parasitic reactances, impedance mismatches, crosstalk, dispersion and frequency-dependent skin losses.

[0024] The clock controller **140** operates from the same input frequency (in this example, 2.4 GHz) and generates clocks for both digital and wireless circuits. The clock controller **140** optimizes speed, power, and radio frequency interference considerations. For example, if the user needs to download a Web cast where data is transmitted to chip from outside wirelessly, the clock controller **140** clocks the system at maximum speed where both the processor and RF circuits are clocked at 2.4 GHz.

[0025] For data going the opposite direction, the needed bandwidth is reduced. Hence, the clock controller **140** divides the 2.4 GHz clock down to a 1.2 GHz clock for the processor. Further, a second order harmonic of the 2.4 Ghz clock signal is used for the RF circuit. The controller **140** can also use the 2.4 GHz with a filter circuit to remove sharp clock edges for RF the circuit.

[0026] The clock controller **140** manages the generation of the clock signals to minimize undesirable EMI emissions that can cause interference. Generally, digital circuits switch quickly between predefined voltage levels, and consequently induce transient disturbances in signal and power lines, as well as energy radiated as electromagnetic waves. A digital circuit switching rapidly but regularly, with edges synchronous to a master clock, can generate noise with a strong spectral component at the clock frequency. Additionally, harmonics at odd multiples of the clock frequency will be generated. If the circuit remains synchronous to a master clock, but switches on random clock edges, spectral components above and below the clock frequency will also be generated. Digital circuits themselves are robust in the presence of noise from other sources. By contrast, analog circuits operate at a multiplicity of voltage levels and frequencies, and are sensitive to induced noise. The noise spectrum produced by dense, high-speed digital circuits can easily interfere with high-frequency analog components. Since the waveforms transitions generated by digital circuits are, at least ideally, step transitions having (in accordance with Fourier analysis) a wide noise bandwidth, potential interference of the chip's digital signals with the chip's analog signals poses a distinct threat to circuit performance.

[0027] In one embodiment, the clock controller **140** generates a processor clock signal at a frequency that is lower